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**Personal Reflection:**

From the module, I’ve learned a lot about how logic circuits work and how a good understanding of logic circuits is vital for computer science. Throughout the labs, I’ve learned to combine both theory and practical to produce a circuit. This helped me a lot as I’m not good with theory but good with practical which solidified the theory in my head. If I was to change anything about the module, it would be the number of classes we had of Digital Logic Design. I would’ve liked to have a few more classes as it would have provided me with more practice with the theory of the logic circuits we were creating. All in all, I really enjoyed the module and learned a lot from the class. My lab reports are the best, in fact I probably messed up with the results, but it has been a huge learning curve for me and I’ve learned so much from my mistakes.

**LAB 1**

**Title:**

NAND LED Circuit

**Date:**

20/NOV/2018

**Aim:**

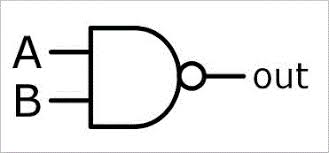
The aim of the experiment is to light up the LED in the circuit using a 7400 Quad 2-input NAND, 8-Way switches and to get used to using the inputs and outputs of a circuit.

**Analysis:**

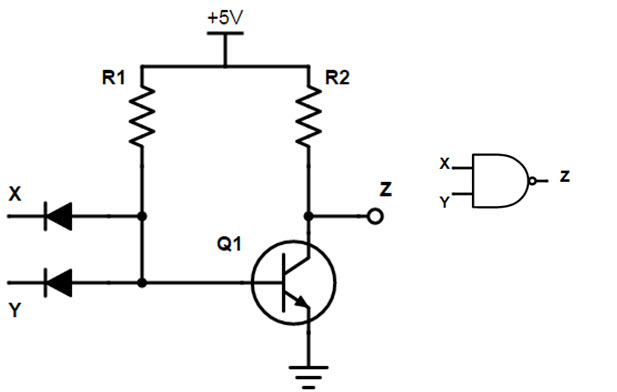
I expected to get a truth table of a NAND gate, (Shown below).

|  |  |  |
| --- | --- | --- |
| **Input** |  | **Output** |
| **A** | **B** | **out** |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**NAND GATE:**

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**Logic Diagram:**

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The logic behind the NAND gate is that if both A and B are on, then the output would be off. Otherwise, the output would be on.

**Results:**

From our lab session we got the following results which matched that of the NAND gate truth table which told us that our results were correct.

|  |  |  |
| --- | --- | --- |
| **Input** |  | **Output** |
| **A** | **B** | **out** |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Conclusion:**

In conclusion, the truth table from our analysis of the circuit diagram matched that of our results. The NAND gate allows current to pass when the inputs are (0,0), (0,1), (1,0). That means that if the LED is off, then the inputs are both on.

**LAB 2**

**Title:**

XOR LED Circuit (using NAND)

**Date:**

1/NOV/2018

**Aim:**

The aim of the experiment is to design and build a circuit that implements a quad NAND 7400 gate (four NAND gates in series) to create a logic gate that resembles an XOR gate.

**Analysis:**

I expected to get a truth table of a XOR gate, (Shown below).

|  |  |  |
| --- | --- | --- |
| **Input** |  | **Output** |
| **A** | **B** | **out** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

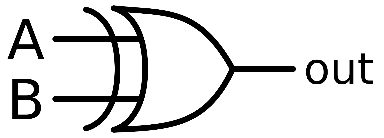
We were able to use DeMorgan’s theorem to establish an equation using only four NAND gates that would resemble the inputs and outputs of an XOR gate.

***F = A’B + AB’***

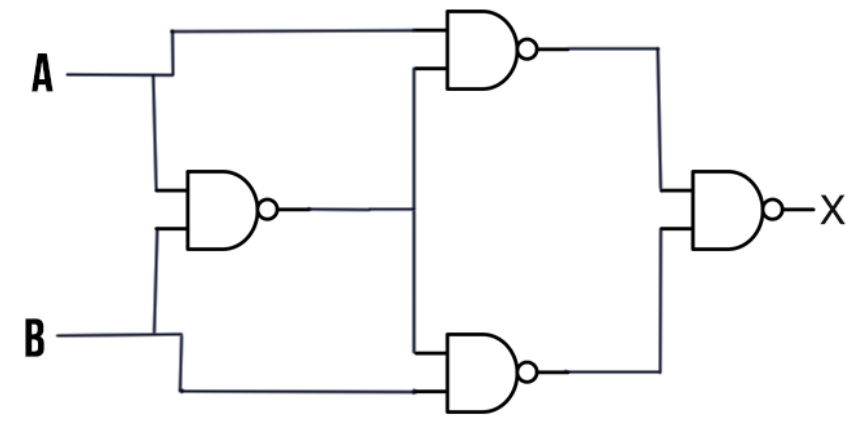
***By Boolean algebra…***

***F = ((A.(A.B)’)’.(B.(A.B)’)’)’***

**XOR GATE:**



**Logic Diagram:**



The logic behind the XOR gate is that if both inputs are either on or off, then the output would be off. Otherwise, the output would be on.

**Results:**

From our lab session we got the following results which matched that of the XOR gate truth table which told us that our results were correct.

|  |  |  |
| --- | --- | --- |
| **Input** |  | **Output** |
| **A** | **B** | **out** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Out = A’B + AB’ + 0 + 0

Out = A’B + AB’ + AA’ + BB’

Out = A(A’ + B’) + B(A’ + B’)

Out = A(AB)’ + B(AB)’

Out’ = [A(AB)’ + B(AB)’]’

Out’ = [A(AB)’ \* (B(AB)’]’

Out’’ = X= [[A(AB)’ \* [B(AB)’]’]’

Out = (A NAND (A NAND B)) NAND (B NAND (A NAND B))

**Conclusion:**

In conclusion, the truth table from our analysis of the circuit diagram matched that of our results. The XOR gate allowed current to pass using 4 NAND gates as shown in the logic diagram. The showed that a XOR gate is just 4 NAND gates, arranged as the logic diagram, would create a XOR gate.

**LAB 3**

**Title:**

Building a circuit using a demultiplexer

**Date:**

29/NOV/2018

**Aim:**

The aim of the experiment is to design, build and test a circuit that uses a 74138 3 to 8-line decoder/demultiplexer and minimal additional circuitry to implement the function:

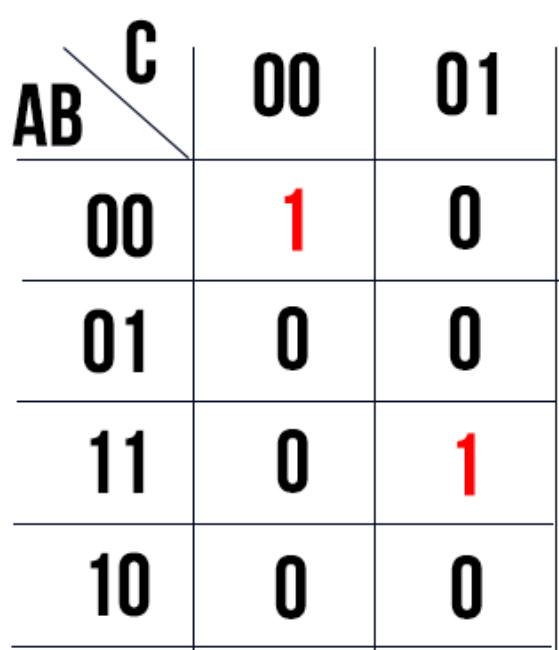
F = x’ y z’ + x z

**Analysis:**

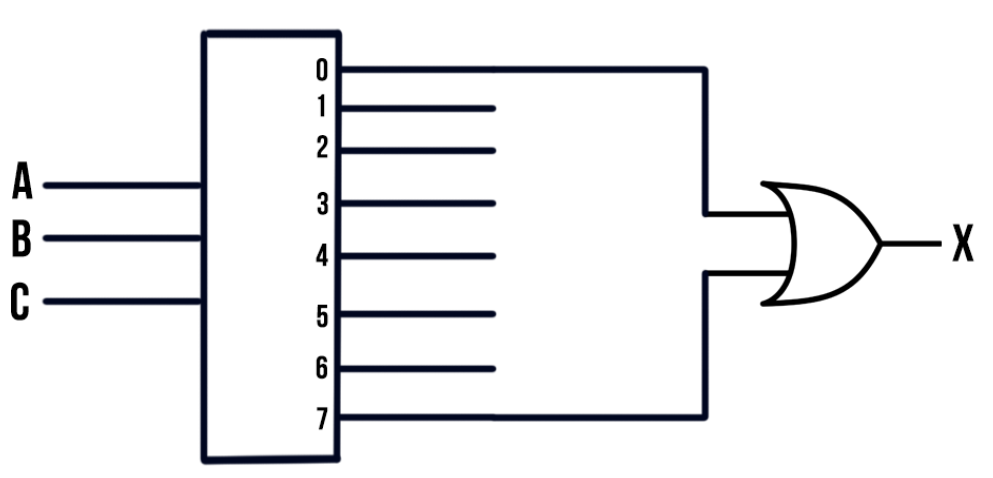
I expected to get a truth table as shown below.

|  |  |  |  |
| --- | --- | --- | --- |
| **Input** |  |  | **Output** |
| **A** | **B** | **C** | **out** |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

**Karnaugh Map:**



**Logic Diagram:**



The logic behind the diagram is that if A, B and C are off, then the output would be on and if A, B and C are on, then the output would remain on. Otherwise, the output would be off.

**Results:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Input** |  |  | **Output** |
| **A** | **B** | **C** | **out** |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Out = A’BC’ + AC

Out = A’BC’ + (AC)\*(B+B’)

Out = A’BC’ + ABC + AB’C

**Conclusion:**

In conclusion, the truth table from our analysis of the circuit diagram matched that of our results. The Karnaugh map (above), matched the results I got.